**SYSTEM DESIGN THROUGH VERILOG**

**Assignment-2**

1. a)Explain about serial data transmission in UART design

b) Write and explain the operation of a 486 BUS model

1. a) write a verilog module for PLA
   1. What is meant by memory interfacing? With suitable diagram explain interfacing memory to a microprocessor
2. a)Write a verilog code for modelling of microcontroller

b) Discuss about RAM cell with neat waveforms and write verilog module for RAM cell

**All final year students submit the Assignment-2 on or before 17-01-2022(Monday) through offline (Hard copy)**